Patent

Attorney Docket No.: Intel 2207/10083
U.S. Serial No.: 09/751,750
Assignee: Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT	:	Talal K. JABER
SERIAL NO.	:	09/751,750
FILED	:	December 29, 2000
FOR	:	MICROPROCESSOR ON-CHIP TESTING ARCHITECTURE AND IMPLEMENTATION
GROUP ART UNIT	:	2133
EXAMINER	:	Guy J. LAMARRE

M/S: APPEAL BRIEFS - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this paper is being facsimile transmitted to the USPTO at (571) 273-8300 or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 17, 2005.

Pilar Rodriguez

ATTENTION: Board of Patent Appeals and Interferences

APPEAL BRIEF

Dear Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on March 17, 2005.

08/19/2005 MBINAS 00000013 110600 09751750
02 FC:1402 500.00 DA

1. REAL PARTY IN INTEREST

The real party in interest in this matter is Intel Corporation. (Recorded December 29, 2000, Reel/Frame 011424/0472).

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings known to Appellant or Appellant's legal representative, which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

3. STATUS OF THE CLAIMS

Claims 1, 3-11 and 13-20 are pending in this application. Claims 1, 3-11 and 13-20 were rejected under 35 U.S.C. §102(b). This appeal is an appeal from the rejection of claims 1, 3-11 and 13-20.

4. STATUS OF AMENDMENTS

Applicant did not make any amendments to the claim subsequent to final rejection. The claims listed on page 1 of the Appendix of this Appeal Brief reflect the present status of the claims (including amendments entered after final rejection).

5. SUMMARY OF THE INVENTION

The embodiment of independent claim 1 of the present invention generally describes an on-chip testing apparatus comprising: a test pattern generator (e.g, reference numeral 11, page 3 line 22) to generate test data for a plurality of testing channels (e.g., 19, page 4, line 3); and a weight selector (e.g., 13, page 3, line 23) coupled to said test pattern generator, said weight selector to store weighting values to bias data for at least one of said testing channels wherein

said weight selector includes a weight storage register (e.g., 115, page 5 line 3) to store said weighting values and said weight selector is to selectively bias individual bits of said test data.

The embodiment of independent claim 9 of the present invention generally describes an on-chip testing apparatus comprising: channel filtering logic (e.g., 17, page 4 line 2) to receive data from a plurality of testing channels (e.g., 19, page 4, line 3), said channel filtering logic to mask output data from a selected testing channel wherein in biasing test data, said biasing is performed selectively on individual bits of said test data.

The embodiment of independent claim 19 of the present invention generally describes a method of performing on-chip testing comprising: receiving data from a plurality of testing channels (e.g., 19, page 4, line 3) at channel filtering logic (e.g., 17, page 4 line 2); and masking output data from a selected testing channel wherein in biasing test data, said biasing is performed selectively on individual bits of said test data.

Referring to Fig. 1, a general block diagram of an LBIST architecture is shown constructed according to an embodiment of the present invention. A pattern generator 11 provides raw data to be input into test circuitry on the chip. A weight selector 13 is coupled to pattern generator 11 to provide a particular weighting of the raw data based on the value in option register 10. The output of the weight selector is supplied to channel data biasing logic 17, which, in turn supplies the data to the LBIST scan channels 19 (e.g., such as those that are known in the art). Clock control & diagnostic logic 21 generates stop and scan clocks for the LBIST scan channels.

Referring to Fig. 2, a more detailed block diagram of the LBIST architecture of Fig. 1 is shown. In this embodiment, the pattern generator is implemented as a pseudo random pattern generator (PRPG) 101 generating a 128-bit value. This value is then fed through a data inverter

register 102, which may be implemented with a set of 128 control-only scan flip-flops to control whether the data going into a certain LBIST channel is inverted or not (as described below). Weight select logic 103 receives the output of the PRPG 101 and data inverter register 102 and weights the bits based on two-bit values supplied by multiplexers 117.

The generation of the S1S2 value starts with the Weight Select Control Register 115 in this embodiment. In this example, the PRPG 101 generates 128 bits (one bit per LBIST channel). Register 115 is a 256 bits wide and these bits are supplied to 128 4:2 multiplexers 117. A weight storage register 115 may be 128 or 256 bits wide depending on the granularity of the biasing of test data within a particular LBIST scan channel. The weight storage register may be loaded and programmed via the JTAG TAP as any other TDR (test data register).

The MUX tree 116 of this embodiment is shown in more detail in Fig. 3. The MUX tree 116 allows addressing within the weight storage register so that all bits within a particular scan segment of an LBIST scan channel are biased. In this embodiment, the select signals (SEL0 to SEL5) mirror the least significant bits of the scan counter 106.

The weighting of the bits from the PRPG 101 and the data inverter register 102 is shown in Fig. 4. Each bit is first ANDed with the S1 bit, then the result is ORed with the S2 bit. If the bits are set to 00, then the corresponding bit from the PRPG 101 would be changed to a 0. If the bits are set to 01, then the corresponding bit from the PRPG 101 would be changed to a 1. A 10 value would leave the bit unchanged (i.e., weighted by ½). If both S1 and S2 are 1, then these bits cause the output of AND gate 41 to output a one and select an output via MUX 43 that is an ANDing of four bits from the PRPG 101. Since the four bits are randomly generated, AND gate 45 will output a 1 on average 1 out of 16 times. Thus, when S1 and S2 are both 1, it results in a weighting of 1/16th. The output of MUX 43 is suppled to an XOR gate 47, which XORs it with

the bit cmd_4D. The value for cmd_4D is controlled by the data inverter register 102. Thus a 1 bit for this particular channel would cause the output of MUX 43 to be inverted by XOR gate 47, and a 0 bit would leave the output of MUX 43 unchanged by XOR gate 47. The outputs of MUX 104 are supplied to the LBIST scan channels 119, and clocked into the appropriate scan channels using the scan clocks.

To generate the inputs to the AND gate 128, an LBIST scan channel segment control register 124 is provided that may be used to address 1 out of 16 segments within an LBIST scan channel. As with the channel decode register, it may be loaded an unloaded via the JTAG port as a TDR register. The 16-bit value from the scan segment register 124 is supplied to a scan channel segment control register 125. Control register 125 is a 16-bit scannable register that is used to control the data compression of 1 out of 16 segments within an LBIST scan channel.

6. ISSUES

A. Are claims 1, 3-8, 11 and 13-18 anticipated by Motika et al. U.S. Patent No. 5,983,380 (hereinafter "Motika")?

B. Are claims 6-8, 9-10, 16-18, 19-20 anticipated by Rajski et al. U.S. Patent No. 6,557,129 (hereinafter "Rajski")?

C. Are claims 9-10, 19-20 rendered obvious by Motika in view of Rajski?

D. Are claims 6-8 and 16-18 rendered obvious by Applicants Admitted Prior Art (hereinafter "AAPA") in view of Swoboda et al U.S. Patent No. 6,349,392 (hereinafter "Swoboda")?

7. ARGUMENT

A. Claims 1, 3-8, 11, and 13-18.

The Office Action asserts that Motika et al. ("Motika") depicts e.g., in Fig. 6 and related description in col. 1 line 25 et seq., the claimed on-chip testing apparatus comprising: a test pattern generator (Fig. 6 Numeral 12, col. 2 line 35) to generate test data for a plurality of testing channels; and a weight selector (Fig. 6 Numerals 118-126 with Numerals 138 and 142, Fig. 5, col. 2 line 35) coupled to said test pattern generator, said weight selector to store weighting values to bias data (e.g., col. 2 line 62) for at least one of said testing channels. The Office Action also asserts Motika et al. depicts, in Fig. 6 and related description in col. 2 line 25 et seq., the claimed apparatus wherein said weight selector includes a weight storage register (Fig. 6 Numerals 118-126 with Numerals 138 and 142, Fig. 5, col. 2 line 35) to store said weighting values and said weight selector is to selectively bias (e.g., col. 2 line 62) individual bits of said test data. Applicants respectfully dissent.

Line 35 of column 2 of Motika discloses a BIST (Built In Self Test) design and a WRP (Weighted Random Pattern) test methodology. Column 2 line 62 of Motika states:

> "These patterns are then biased or weighted to optimize them for a specific logic design.

Applicant respectfully submits that nowhere in Motika (including the Figures and cited sections) is the disclosure, teaching or suggestion of at least the limitation "...wherein said weight selector includes a weight storage register to store said weighting values and said weight selector is to *selectively bias individual bits of said test data*" as claimed in the embodiment of amended claim 1. A generic disclosure of a biasing capability is not sufficient to disclose the

ability to selectively bias individual bits of test data. Further support can be found in the specification at page 5 line 12, which states:

> "The biasing values can be determined by running the existing Weighted Pattern Test generation algorithms, which are well know in the art. The weight storage register can also be useful in forcing a segment of an LBIST scan channel to a deterministic value every time a scan load takes place. *In other words, each bit of the segment can be set to a desired value*" (*emphasis added*).

The Advisory Action further asserts that Motika does disclose equivalent test weighting/biasing with register means in Fig. 4 wherein Numeral 12 generates test data that is applied to WRP 144 to be biased/weighed as described in col. 5 line 3 et seq. and col. 6 line 3 et seq., said biasing being effected selectively on the plural applied test bits from *Numeral 12*. See Fig. 4 *Numeral 144* for additional weight distribution forced onto output of *Numeral 12* with related register/storage means.

Column 5 line 3 of Motika states:

> Each test can then be applied multiple times for each weight set, where the weight set consists of assigning a weight factor or probability to each SRL. The weight factor is typically of binary granularity with probabilities of "1" equal to 1/32, 1/16, 1/8, 1/4, 1/2, 3/4, 7/8, 5/16, or 31/32.

This paragraph discloses the selection of a weight factor during the testing procedure, but does not disclose the ability of a weight selector is to *selectively bias individual bits of said test data.*

Column 6 line 3 states:

> The WRP generation function block 144 shown in FIG. 4 can be implemented with only a few logic blocks. Reference numerals utilized in FIG. 4 which are like, similar or identical to reference numerals utilized in FIG. 3 indicate like, similar or identical components. Block 144 obtains its input from LFSR 12 outputs, all of which generate P{1}=1/2 pseudo random patterns. By logically gating these LFSR 12 outputs the probabilities can be modified to any desired values. In the example shown, a very simple binary granularity probability weights are shown. Two XOR gates 148, 150 generate the p or 1-p complement probability signal as determined by the SRI bit. 4:1 MUX 146

> selects the desired WFP. The logic circuit shown in FIG. 4 is intended to convey the concept, the actual implementation could be somewhat different depending on the technology, timing requirement, and other design considerations.

The cited paragraph only describes the generation of the weighted random pattern function, wherein outputs are obtained and gated to derive desired probability values. Once again, however, there is no disclosure of the ability of a weight selector is to *selectively bias individual bits of said test data.*

Applicants respectfully submit that since each and every limitation of the claimed embodiment is not covered by cited references, the 102(b) rejection is lacking and should be withdrawn. Independent claim 11 contains substantively similar limitations, and therefore the 102(b) rejection for these claims should be withdrawn as well. Claims 3-8 and 13-18 depend from independent claims 1 and 11, and therefore should be allowed as well.

B. Claims 6-8, 9-10, 16-18, 19-20.

Second, Applicant additionally submits that Rajski et al. ("Rajski") does not teach, suggest or disclose "[a]n on-chip testing apparatus comprising: channel filtering logic to receive data from a plurality of testing channels, said channel filtering logic to mask output data from a selected testing channel wherein in biasing test data, *said biasing is performed selectively on individual bits of said test data*" (as in amended claim 9).

The Office Action states that Rajski's Fig. 6 anticipates such claims because scan chains 44 are effectively blocked or masked via control block 46 prior to compaction by block 48 (also refer to Fig. 10 for logic implementation, also to col. 3 line 12, col. 13 lines 41-49 and col. 7 line 41 et seq., and MISR in Fig. 2: Block 22) and Fig. 14: Block 176. Applicants respectfully dissent. Column 3 line 12 states:

> "[a]n ideal compaction algorithm has the following features: (1) it is easy to implement as a part of the on-chip test circuitry, (2) it is not a limiting factor with respect to test time, (3) it provides a logarithmic compression of the test data, and (4) it does not lose information concerning faults".

This section describes the goals of a compaction algorithm but not the ability of a testing apparatus to bias selectively on individual bits of test data.

Column 13 lines 41-49 state:

> "[a] method for selectively compacting test responses of an integrated circuit, comprising: passing N test responses in an integrated circuit to a selector circuit; using the selector circuit, selectively preventing between 0 and N of the test responses from being passed to a compactor while allowing the remaining test responses to be passed to the compactor; and compacting the test responses passed to the compactor by the selector circuit; controlling the selector circuit via an external ATE".

This section generically describes some steps used in compacting test responses but again does not disclose the ability of a testing apparatus to bias selectively on individual bits of test data during a testing process.

Column 7 line 41 states:

> "[a]lthough FIG. 10 shows only a single control line, additional control lines can be used to mask different groups of scan chains".

Here, the Rajski reference describes the ability to add control during a *masking* process, not a *biasing* process as described in the embodiment of claim 9.

Lastly, the description of Block 176 states:

> In process block 176, the selector circuit controls which test responses are masked. In particular, the selector circuit controls which scan chains are masked or which bits in the scan chains are masked. For example, in FIG. 8, the selector circuit *masks* the entire scan chain that is identified in the scan identification field 58. In FIG. 10, only individual bits of a scan chain are *masked*. In any event, in process block 176, the selector circuit typically masks unknown data or multiple fault effects so that the desired fault effect can propagate to the output (in some modes of operation, all of the test responses may pass to the output). In the event that the selector circuit includes a control register, the control

register may be loaded concurrently with loading the test patterns in the scan chains or it can be loaded prior to reading the test responses.

Here, the Rajski reference generically describes the *masking* process. A selector circuit controls the masking process by directing the masking of a chain identified in the scan identification field. The Rajski reference further discloses the that individual bits in a scan chains may be *masked.*

The Advisory Action further remarks that Rajski does disclose equivalent channel filtering logic along with test response masking means in Fig. 14: *Block 176* (as reproduced below at page 5 of instant final rejection), wherein a channel selecting/filtering logic *masks* undesired test responses or undesired bits of the test responses. Subsequently, desired test responses are passed to be compressed via MISR in Block 178. Regardless, the Applicants argument still stands that nowhere in Rajski (including the Figures and cited sections discussed immediately above) is the disclosure, teaching or suggestion of at least the limitation "...wherein in biasing test data, *said biasing* is performed selectively on individual bits of said test data" as claimed in the embodiment of amended claim 9. Applicants submit independent claims 6, 16 and 19 contain similar allowable limitations, and dependent claims 7-8, 10, 17-18 and 20 are allowable as they depend from allowable base claims.

C. Claims 9-10, 19-20

Third, the Office Action rejects claims 9-10 and 19-20 under 35 U.S.C. 103 (a) as being unpatentable over Motika in view of Rajski. The Office Action states:

> As per Claims 9, 19, Motika et al. substantially depicts, in Fig. 6 and related description in col. 2 line 25, the claimed on-chip testing apparatus comprising: channel filtering logic to receive data from a plurality of testing channels, said channel filtering logic to select or mask output data from a selected testing channel, e.g., in Fig. 6: MUX receives inputs from left-most BS chain and right-most SRL chain to effect selection control to MISR. Not specifically described in detail in Motika et al. is the step of output data masking.

However Rajski et al., in an analogous art, discloses a testing methodology wherein such techniques are described. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in Motika et al. by including therein output data masking means as taught by Rajski et al., because such modification would provide the procedure disclosed in Motika et al. with a technique wherein "undesirable test output data is concealed." (see Rajski et al., col. 4 lines 43-47)

As per Claims 10, 20, Motika et al. depicts, in Fig. 6 and related description in col. 2 line 25 et seq., the claimed apparatus further comprising: a signature register coupled to said channel filtering logic to receive said data e.g., in Fig. 6: MUX receives inputs from left-most BS chain and right-most SRL chain to effect selection control to MISR.

Column 2 line 25 states:

"[w]hile the prior art testing methods were suitable for testing devices of the then-existing complexity, the increase in circuit density requires more sophisticated testing techniques, not only to reduce testing time, but to assure the functional integrity of these devices".

Column 4 lines 43-47 state:

"[g]enerally, the present invention combines a flat random BIST structure and a modified WRP concept into an extended BIST design. This design integrates on-chip the weighted pattern generation with external weight selection".

However, Applicant again respectfully submits that neither Rajski nor Motika teach, suggest or disclose anywhere "[a]n on-chip testing apparatus comprising: channel filtering logic to receive data from a plurality of testing channels, said channel filtering logic to mask output data from a selected testing channel wherein in biasing test data, *said biasing is performed selectively on individual bits of said test data*" (as in amended claim 9). As detailed above, both Rajski and Motika contain deficiencies making them unable to support a proper 35 U.S.C. 102 rejection. They both fail to make up for each other's deficiencies and therefore cannot be properly combined to serve as the basis of a 35 U.S.C. 103(a) rejection. Since each and every limitation is not covered by the cited prior art, the 103 (a) rejection is lacking and should be

withdrawn. Amended independent claim 19 contains substantively similar limitations and is allowable for similar reasons. Claims 10 and 20 depend from allowable independent claims and therefore should be allowed as well.

D. Claims 6-8 and 16-18.

Lastly, the Office Action rejects claims 6-8 and 16-18 under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Swoboda et al. ("Swoboda"). It states:

> As per Claims 6-8, 16-18, Admitted prior art substantially discloses the claimed the claimed on-chip testing means comprising; ... Not specifically described in detail in Admitted prior art is the step of clock stopping means along with associated hardware for implementation thereof. However Swoboda et al., in an analogous art, discloses a testing methodology in "*Devices, systems and methods for mode driven stops,* "wherein such techniques are described.

Column 14 lines 14-27 state:

> The analysis circuitry includes condition sensors such as hardware breakpoint sensors for controlled stops and tract stack circuitry for real-time trace recordkeeping. The analysis circuitry is serial-scan accessible and designated the analysis domain 1217. All peripherals including memory and serial and parallel ports are denominated as the system domain 1215. For uniformity of description, JTAG control 1201 is regarded as a clock domain also in which test clock JCLK is active. Emulation control circuitry 1203 is a further domain of FIG. 32. Special message passing circuitry 1216 is also included in the system or analysis domain, to even more fully use the host computer 1101 as an attached processor by interfacing the TIBUS to the serial scan line 1103 of FIG. 45. FIG. 53 shows a physical perspective of the various domains on the chip of device 11.

Column 20 line 9 states:

> Data and control information are scanned into and out of the domains on test clock JCLK, and the domains are independently and selectively started on functional clock FCLK and stopped, in extensive sequences to accomplish emulation, simulation and test functions with a wide degree of flexibility as circumstances of the development, manufacturing and field environments dictate.

However, Applicant again respectfully submits that neither Applicant's Admitted prior art nor Swoboda teach, suggest or disclose "[a] method of performing on-chip testing

comprising: selectively supplying functional clocking signals to a plurality of testing channels to operate logic in said testing channels wherein in biasing test data, said biasing is performed selectively on individual bits of said test data" (as in amended claim 16). Therefore since neither the Applicant's Admitted prior art nor Swoboda teach, suggest or disclose at least the claimed limitation "*...wherein in biasing test data, said biasing is performed selectively on individual bits of said test data*", the combination of both does not either. Since each and every limitation is not covered by the cited prior art, the 103 (a) rejection is lacking and should be withdrawn. Amended independent claim 6 contains substantively similar limitations and is allowable for similar reasons. Claims 7-8 and 17-18 depend from allowable independent claims and therefore should be allowed as well.

Appellants therefore respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's decision rejecting claims 1, 3-11, and 13-20 and direct the Examiner to pass the case to issue.

The Examiner is hereby authorized to charge the appeal brief fee of **$500.00** and any additional fees which may be necessary for consideration of this paper to Kenyon & Kenyon Deposit Account No. **11-0600.**

Respectfully submitted,

KENYON & KENYON

Date: August 17, 2005

By: _____
Sumit Bhattacharya
(Reg. No. 51,469)

KENYON & KENYON
333 West San Carlos St., Suite 600
San Jose, CA 95110
Telephone: (408) 975-7500
Facsimile: (408) 975-7501
68714.1

8. APPENDIX

(Brief of Appellants Talal K. Jaber
U.S. Patent Application Serial No. 09/750,150)

CLAIMS ON APPEAL

1. (Previously presented) An on-chip testing apparatus comprising:

a test pattern generator to generate test data for a plurality of testing channels; and

a weight selector coupled to said test pattern generator, said weight selector to store weighting values to bias data for at least one of said testing channels wherein said weight selector includes a weight storage register to store said weighting values and said weight selector is to selectively bias individual bits of said test data.

2. (Cancelled)

3. (Previously Presented) The apparatus of claim 1 wherein said weight selector causes a reduction in power usage when said weight storage registers store weighting values to bias data for at least one testing channels to one of all 0 values and all 1 values.

4. (Previously presented) An on-chip testing apparatus comprising:

a test pattern generator to generate test data for a plurality of testing channels;

clock control logic to selectively supply scan clocking signals to said testing channels, such that said scan clocking signals scan said test data into said testing channels wherein in biasing test data, said biasing is performed selectively on individual bits of said test data.

5. (Original) The apparatus of claim 4 further comprising:

a signature register coupled to said testing channels to receive data from said testing channels when said scan clocking signals are supplied to said testing channels.

6. (Previously presented) An on-chip testing apparatus comprising:

clock control logic to selectively supply functional clocking signals to a plurality of testing channels, such that said functional clocking signals operate logic in said testing channels wherein in biasing test data, said biasing is performed selectively on individual bits of said test data.

7. (Original) The apparatus of claim 6 wherein said clock control logic further includes clock control logic to generate stop clock signals to said testing channels.

8. (Original) The apparatus of claim 7 wherein said clock control logic further includes a scan counter counting said functional clocking signals and a breakpoint stop register to store a value such that at least one of said stop clock signals is generated when a count in said scan counter matches a value in said breakpoint stop register.

9. (Previously presented) An on-chip testing apparatus comprising:

channel filtering logic to receive data from a plurality of testing channels, said channel filtering logic to mask output data from a selected testing channel wherein in biasing test data, said biasing is performed selectively on individual bits of said test data.

10. (Original) The apparatus of claim 9 further comprising:

a signature register coupled to said channel filtering logic to receive said data.

11. (Previously presented) A method of performing on-chip testing comprising:

generating test data in a test pattern generator for a plurality of testing channels; and

biasing said test data for at least one of the testing channels with weighting values stored in a weight selector coupled to said test pattern generator wherein said biasing is performed selectively on individual bits of said test data.

12. (Cancelled)

13. (Previously presented) The method of claim 11 wherein in biasing said test data all of said test data is biased to one of all 0 values and all 1 values.

14. (Previously presented) A method of performing on-chip testing comprising:

generating test data in a test pattern generator for a plurality of testing channels; and

selectively supplying scan clocking signals to said testing channels to scan said test data into said testing channels wherein in biasing test data, said biasing is performed selectively on individual bits of said test data.

15. (Original) The method of claim 14 further comprising:

supplying said data received from said testing channels to a signature register coupled to said testing channels.

16. (Previously presented) A method of performing on-chip testing comprising:

selectively supplying functional clocking signals to a plurality of testing channels to operate logic in said testing channels wherein in biasing test data, said biasing is performed selectively on individual bits of said test data.

17. (Original) The method of claim 16 further comprising:

selectively generating stop clock signals to said testing channels.

18. (Original) The method of claim 17 further comprising:

counting said functional clocking signals in a scan counter; such that at least one of said stop clock signals is generated when a count in said scan counter matches a value in a breakpoint stop register.

19. (Previously presented) A method of performing on-chip testing comprising:

receiving data from a plurality of testing channels at channel filtering logic; and

masking output data from a selected testing channel wherein in biasing test data, said biasing is performed selectively on individual bits of said test data.

20. (Original) The method of claim 19 further comprising:

supplying masked output data from said channel filtering logic to a signature register coupled to said channel filtering logic.

9. EVIDENCE APPENDIX

No further evidence has been submitted with this Appeal Brief.

10. RELATED PROCEEDINGS APPENDIX

Per Section 2 above, there are no related proceedings to the present Appeal.